

# FMJ LG PC Card



## OVERVIEW

The Last Generation FMJ PC Card is a small, low cost, high performance, removable solid-state memory storage subsystem. It is an appropriate replacement for legacy hard disk drives and host systems that require low power and small scalable storage solutions. FMJ technology is designed for customer's that prefer reliable operation in harsh environments and a long product lifecycle. Amongst the endless number of applications are networking products, military systems, interactive kiosks, record and playback systems, medical equipment, industrial control systems, avionics, and voting machines.

## FEATURES

- Capacity range: 32MB to 8GB
- Industry standard Type II PC Card form factor
- Integrated wear-leveling and ECC technology
- Supports both 8-bit and 16-bit data register transfers
- Supports dual-voltage 3.3V or 5V interface
- MTBF >4,000,000 hours
- ATA-3 compliant
- Supports PIO modes 0-4 and multi-word DMA modes 0-2
- RoHS 6 of 6 compliant
- Industrial temperature version available



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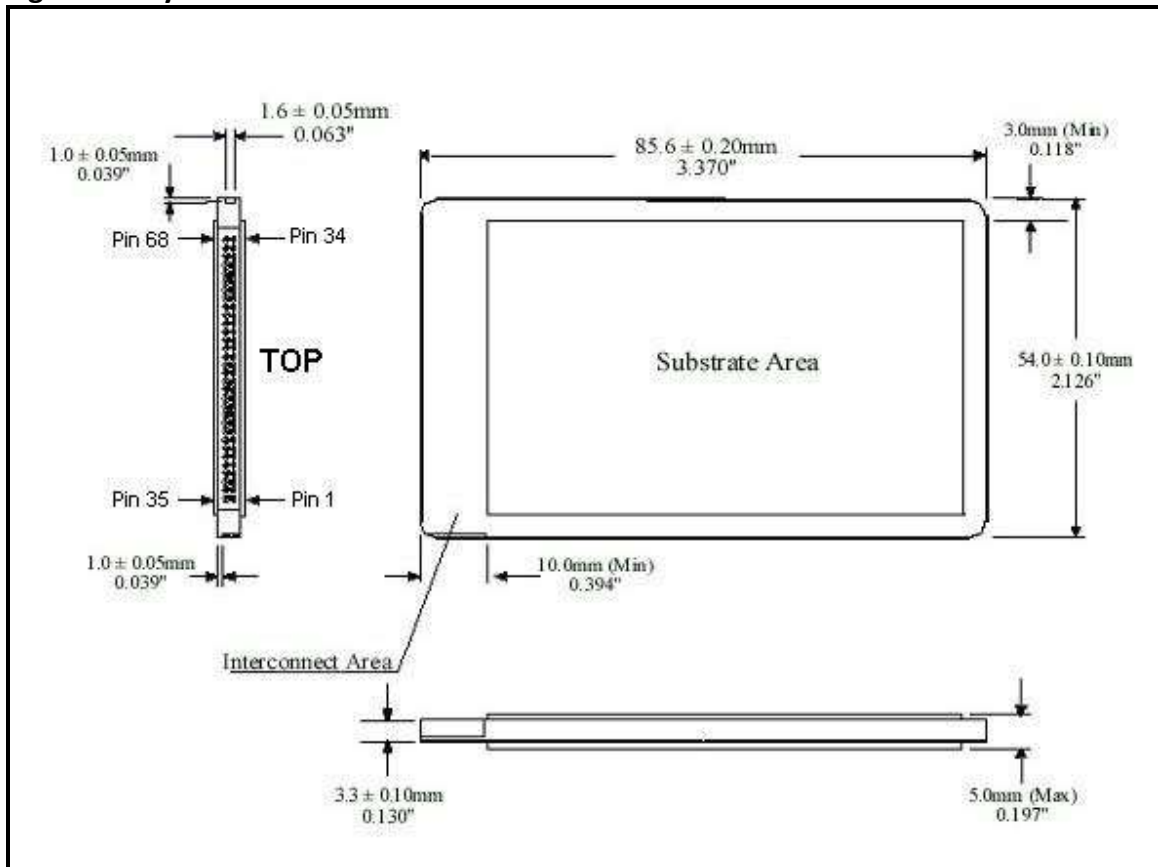
## 1.0 Physical Specifications

The FMJ PC Card products are offered in an Industry Standard Type II form factor.

### 1.1 Physical Dimensions

The following figure describes the physical dimensions for the FMJ PC Card.

**Figure 1. Physical Dimensions**





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## 2.0 Product Specifications

**Note:** All FMJ PC Card values quoted are typical at 25°C and nominal supply voltage.

### 2.1 System Performance

Table 1 shows the System Performance characteristics of the FMJ PC Card.

**Table 1: System Performance**

Parameter	Value
Reset to Ready (max)	400ms
Command to DRQ (max)	2ms
Read Transfer Rate	Up to 8MB/s
Write Transfer Rate	Up to 6MB/s
Burst Transfer Rate	16.7MB/s

### 2.2 Reliability

Table 2 shows the Reliability information on the FMJ PC Card.

**Table 2: Reliability Information**

Parameter	Value
MTBF (@ 25°C)	4,000,000 hours
Bit Error Rate	<1 non-recoverable error in 10 <sup>15</sup> bits read
Data Retention	10 Year

### 2.3 Capacity

Table 3 shows the Product Capacities of the FMJ PC Card.

**Table 3: Product Capacity**

Product Capacity	Formatted Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors
32MB	32,112,640	62,720	490	4	32
64MB	64,225,280	125,440	490	8	32
128MB	130,154,496	254,208	993	8	32
256MB	260,571,136	508,928	994	16	32
512MB	521,773,056	1,019,088	1011	16	63
1GB	1,047,674,880	2,046,240	2030	16	63
2GB	2,098,446,336	4,098,528	4066	16	63
4GB	4,224,761,856	8,251,488	8186	16	63
8GB	8,455,200,768	16,514,064	16383*	16	63



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## 2.4 Environmental

**Table 4: Environmental Specifications**

Temperature (Operating)	0°C to 70°C (Commercial) -40°C to 85°C (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

## 3.0 Electrical Specifications

### 3.1 Absolute Maximum Ratings

**Table 5: Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	Ts	-55	125	°C
Operating Temperature*	TA	-40	85	°C
Supply Voltage Relative to Ground	Vcc	-0.3	6.0	V
Input/Output Voltage	Vio	-0.3	Vcc + 0.3	V

\* = Industrial temperature version.

### 3.2 DC Specifications

**Table 6: DC Specifications**

Parameter	Symbol	3.3V		5.0V		Units
		Min	Max	Min	Max	
Supply Voltage	Vcc	3.00	3.60	4.5	5.5	V
Input Leakage Current	ILI	-	10	-	10	µA
Output Leakage Current	ILO	-	10	-	10	µA
Icc Read Current	ICCR	-	75	-	100	mA
Icc Write Current	ICCW	-	75	-	100	mA
Icc Standby Current	ICCS	-	0.5	-	1.0	mA
Input Low Voltage	VIL	-0.3	Vcc x 0.3	-0.3	Vcc x 0.3	V
Input High Voltage	VIH	Vcc x 0.7	Vcc + 0.3	Vcc x 0.7	Vcc + 0.3	V
Output Low Voltage	VOL	-	0.4	-	0.4	V
Output High Voltage	VOH	Vcc - 0.4	-	Vcc - 0.4	-	V

## 3.2 Pin Assignments/Signals

Table 7 describes the FMJ PC Card connector assignments and signals. Refer to the PC Card specification for more information on the signals.

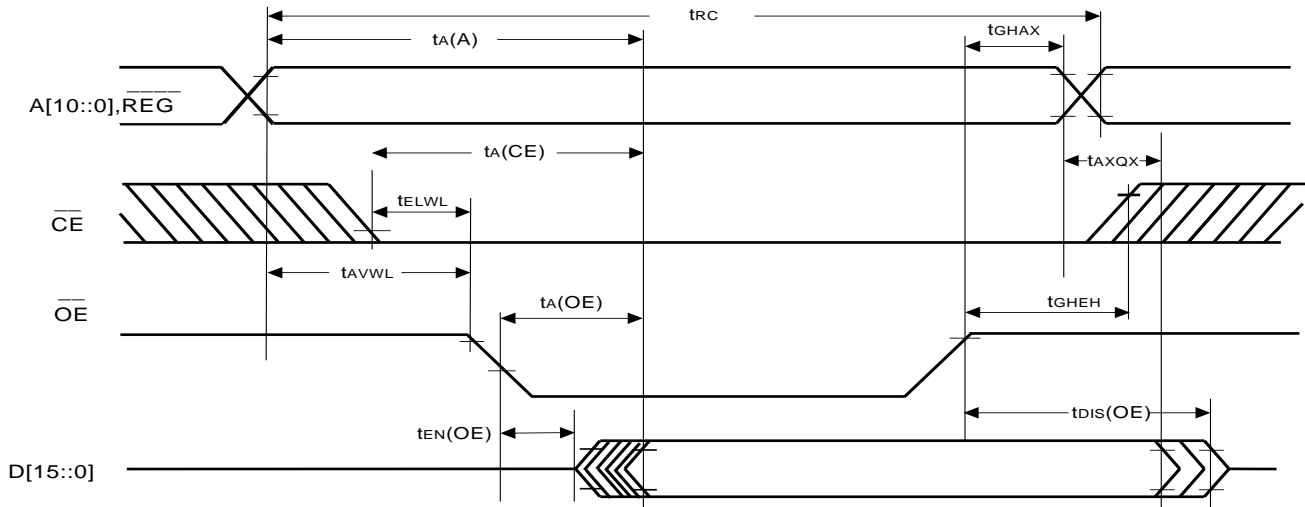
**Table 7: Pin Assignments**

Pin	Memory Mode	I/O Mode	IDE-ATA Mode	Pin	Memory Mode	I/O Mode	IDE-ATA Mode
1	GND	GND	GND	35	GND	GND	GND
2	D3	D3	D3	36	CD1#	CD1#	CD1#
3	D4	D4	D4	37	D11	D11	D11 <sup>1</sup>
4	D5	D5	D5	38	D12	D12	D12 <sup>1</sup>
5	D6	D6	D6	39	D13	D13	D13 <sup>1</sup>
6	D7	D7	D7	40	D14	D14	D14 <sup>1</sup>
7	CE1#	CE1#	CS0#	41	D15	D15	D15 <sup>1</sup>
8	A10	A10	A10	42	CE2#	CE2#	CS1#
9	OE#	OE#	ATA-SEL#	43	VS1#	VS1#	VS1#
10	NC	NC	NC	44	IORD#	IORD#	IORD#
11	A9	A9	A9	45	IOWR#	IOWR#	IOWR#
12	A8	A8	A8	46	NC	NC	NC
13	NC	NC	NC	47	NC	NC	NC
14	NC	NC	NC	48	NC	NC	NC
15	WE#	WE#	WE#	49	NC	NC	NC
16	RDY/BSY	IREQ#	INTRQ	50	NC	NC	NC
17	VCC	VCC	VCC	51	VCC	VCC	VCC
18	NC	NC	NC	52	NC	NC	NC
19	NC	NC	NC	53	NC	NC	NC
20	NC	NC	NC	54	NC	NC	NC
21	NC	NC	NC	55	NC	NC	NC
22	A7	A7	A7	56	CSEL#	CSEL#	CSEL#
23	A6	A6	A6	57	VS2#	VS2#	VS2#
24	A5	A5	A5	58	RESET	RESET	RESET#
25	A4	A4	A4	59	WAIT#	WAIT#	IORDY
26	A3	A3	A3	60	INPACK#	INPACK#	DMARQ
27	A2	A2	A2	61	REG#	REG#	DMACK#
28	A1	A1	A1	62	BVD2	SPKR#	DASP#
29	A0	A0	A0	63	BVD1	STSCHG#	PDIAG#
30	D0	D0	D0	64	D8	D8	D8 <sup>1</sup>
31	D1	D1	D1	65	D9	D9	D9 <sup>1</sup>
32	D2	D2	D2	66	D10	D10 <sup>1</sup>	D10 <sup>1</sup>
33	WP	IOIS16#	IOCS16#	67	CD2#	CD2#	CD2#
34	GND	GND	GND	68	GND	GND	GND

1 = These signals are required only for 16-bit access, and not required when installed in 8-bit systems.

## 3.3 Signal Timing

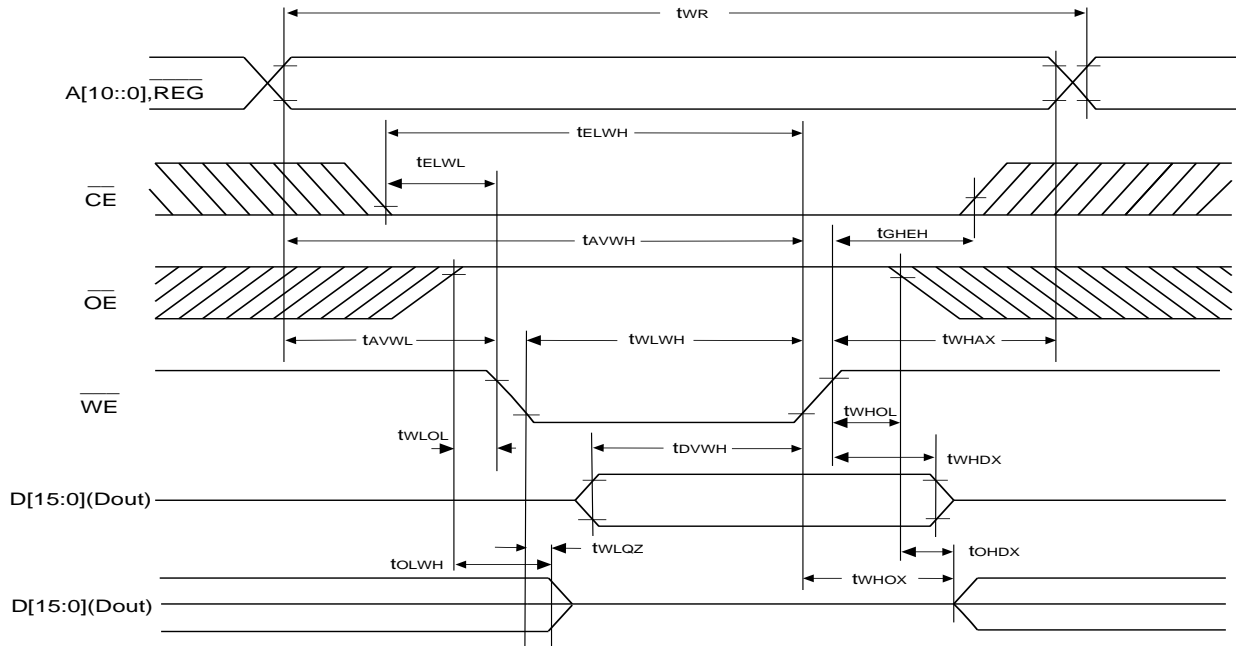
### 3.3.1 Attribute & Common Memory Read Timing



Symbol	Parameter	Min	Max	Units
$t_{RC}$	Read Cycle Time	150		nsec
$t_{A(A)}$	Address Access Time	-	100	
$t_{A(CE)}$	Card Enable Access Time	-	100	
$t_{A(OE)}$	Output Enable Access Time	-	50	
$t_{DIS(OE)}$	Output Disable Time from OE	-	50	
$t_{EN(OE)}$	Output Enable Time from OE	5	-	
$t_{AXQX}$	Data Valid from Address Change	0	-	
$t_{AVWL}$	Address Setup Time	10	-	
$t_{AXQX}$	Address Hold Time	15	-	
$t_{ELWL}$	Card Enable Setup Time before OE	0	-	
$t_{GHEH}$	Card Enable Hold Time following OE	15	-	

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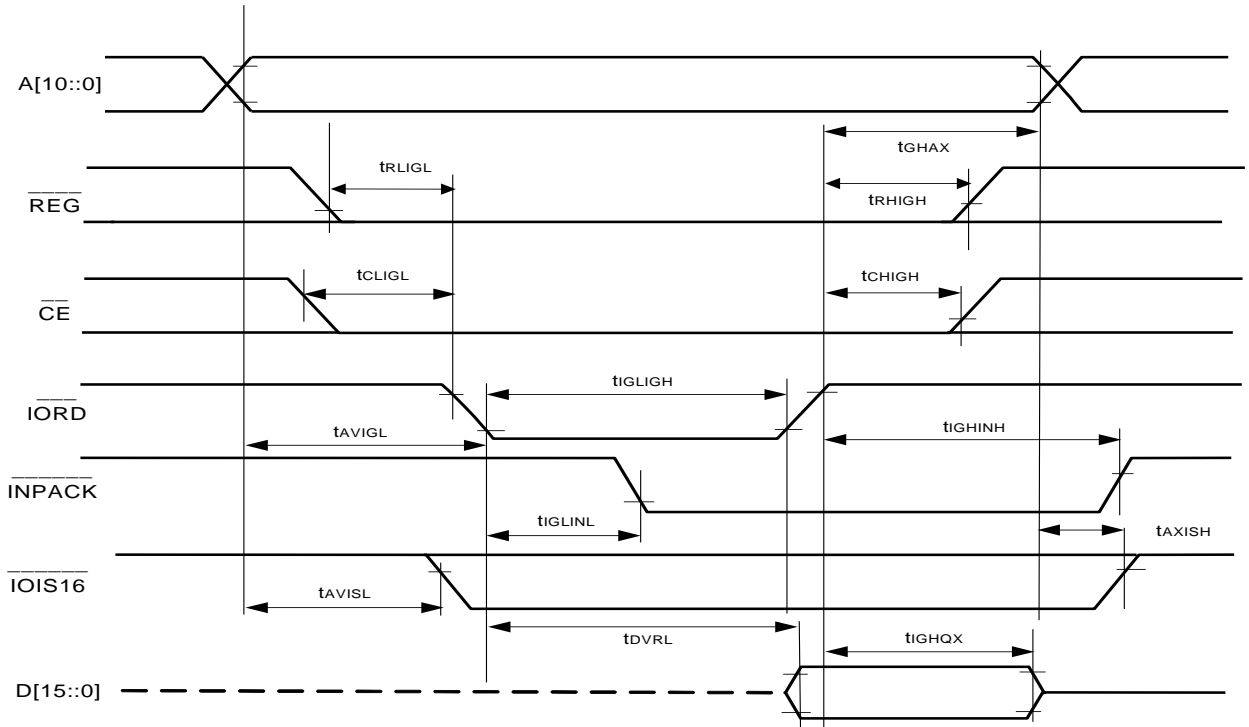
## 3.3.2 Attribute & Common Memory Write Timing



Symbol	Parameter	Min	Max	Units
$t_{WR}$	Write Cycle Time	150	-	nsec
$t_{WLWH}$	Write Pulse Width	60	-	
$t_{AVWL}$	Address Setup Time	10	-	
$t_{AVWH}$	Address Setup Time for WE	70	-	
$t_{ELWH}$	Card Enable Setup Time for WE	70	-	
$t_{WHDX}$	Data Hold Time	10	-	
$t_{WHAX}$	Write Recover Time	15	-	
$t_{WLQZ}$	Output Disable Time from WE	-	75	
$t_{OLWH}$	Output Disable Time from OE	-	100	
$t_{WHOX}$	Output Enable Time from WE	5	-	
$t_{OHDX}$	Output Enable Time from OE	5	-	
$t_{WLOL}$	Output Enable Setup for WE	10	-	
$t_{WHOL}$	Output Enable Hold from WE	10	-	
$t_{ELWL}$	Card Enable Setup Time before WE	0	-	
$t_{GHEH}$	Card Enable Hold Time from WE	15	-	
$t_{DVWH}$	Data Setup Time	40	-	



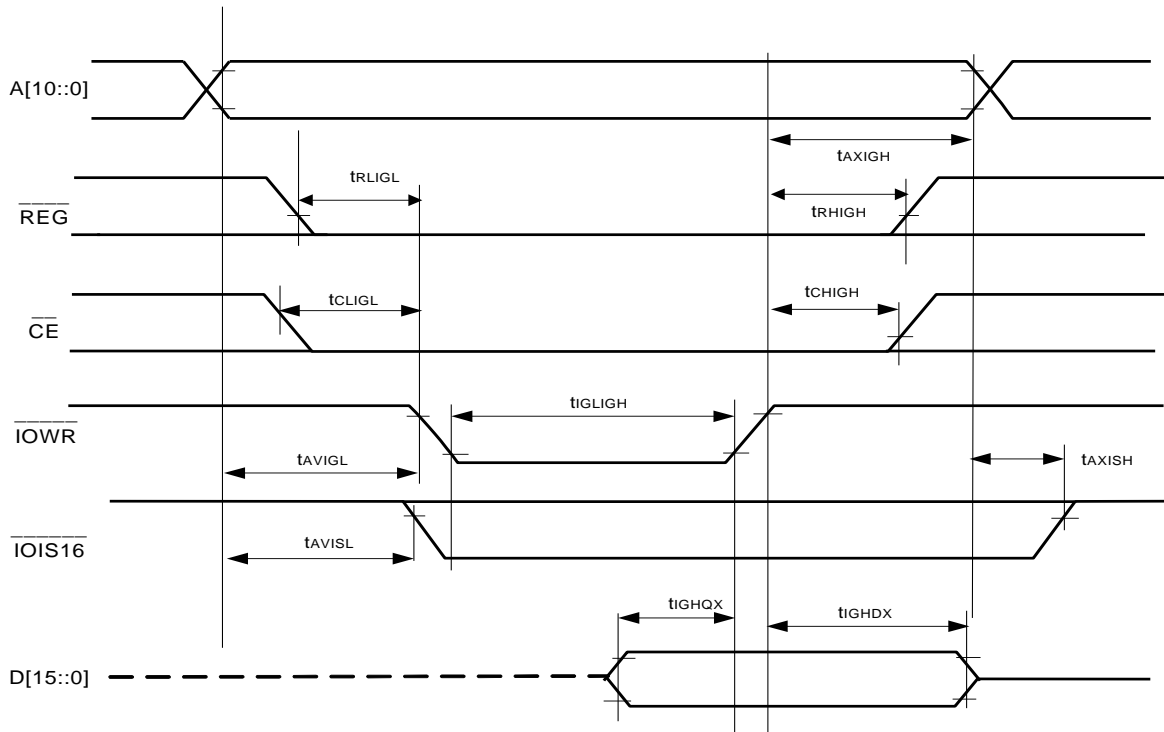
## 3.3.3 I/O Access Read Timing



Symbol	Parameter	Min	Max	Units
t <sub>DVRL</sub>	Data Delay after IORD	-	50	nsec
t <sub>GHQX</sub>	Data Hold following IORD	5	-	
t <sub>GLIGH</sub>	IORD Pulse Width	65	-	
t <sub>AVIGL</sub>	Address Setup before IORD	25	-	
t <sub>GHAX</sub>	Address Hold following IORD	10	-	
t <sub>CLIGL</sub>	CE Setup before IORD	5	-	
t <sub>CHIGH</sub>	CE Hold following IORD	10	-	
t <sub>RLIGL</sub>	REG Setup before IORD	5	-	
t <sub>RHIGH</sub>	REG Hold following IORD	0	-	
t <sub>GLINL</sub>	INPACK Delay falling from IORD	-	(1)	
t <sub>GHINH</sub>	INPACK Delay Rising from IORD	-	(1)	
t <sub>AVISL</sub>	IOIS16 Delay Falling from Address	-	(1)	
t <sub>AXISH</sub>	IOIS16 Delay Rising from Address	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

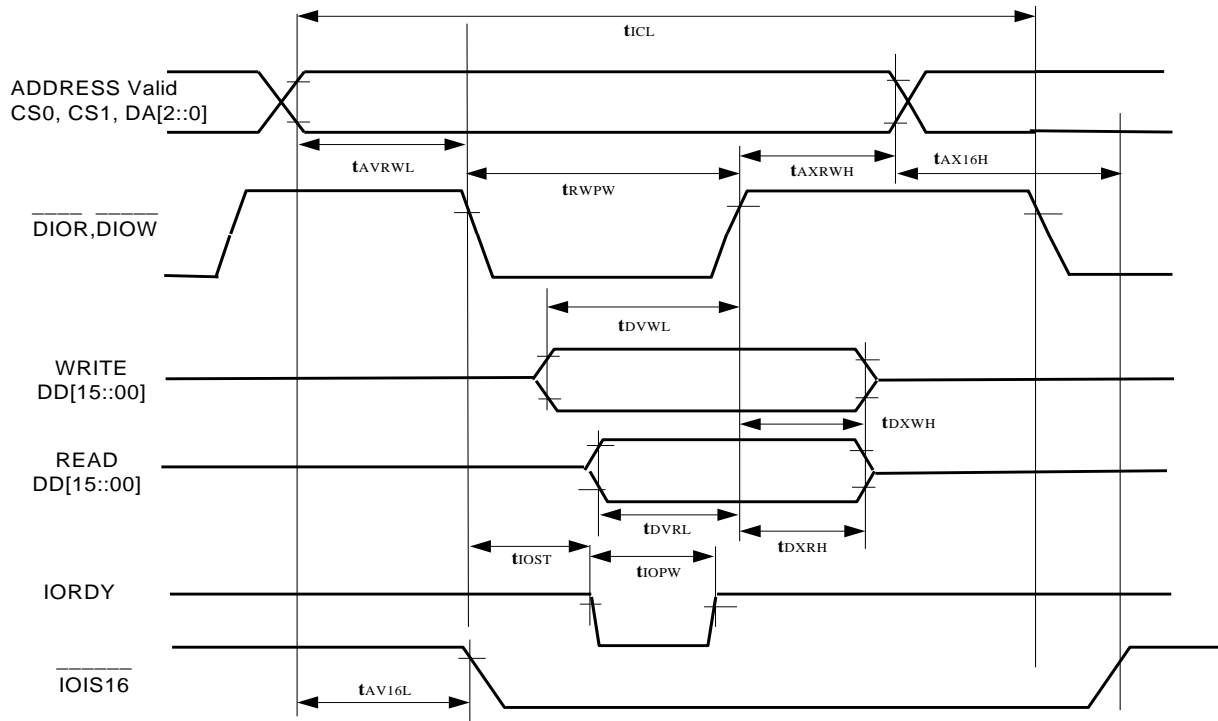
## 3.3.4 I/O Access Write Timing



Symbol	Parameter	Min	Max	Units
tIGHDX	Data Hold following IOWR	5	-	nsec
tIGHQX	Data Setup before IOWR	20	-	
tIGLGH	IOWR Pulse Width	65	-	
tAVIGL	Address Setup before IOWR	25	-	
tAXIGH	Address Hold following IOWR	10	-	
tCLIGL	CE Setup before IOWR	5	-	
tCHIGH	CE Hold following IOWR	10	-	
tRLIGL	REG Setup before IOWR	5	-	
tRHIGH	REG Hold following IOWR	0	-	
tAVISL	IOIS16 Delay Falling from Address	-	(1)	
tAXISH	IOIS16 Delay Rising from Address	-	(1)	

**Note: 1) IOIS16 and INPACK is not supported.**

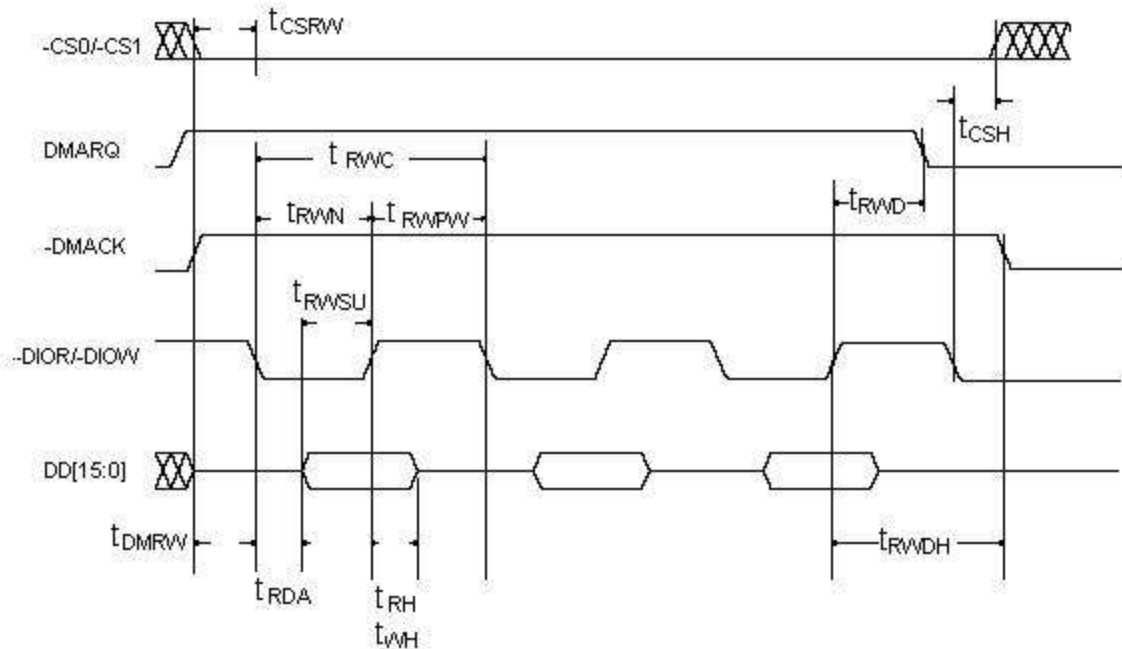
## 3.3.5 True IDE Read/Write Access Timing



Symbol	Parameter	Min	Max	Units
t <sub>ICL</sub>	Cycle Time	100	-	nsec
t <sub>AVRWL</sub>	Address Valid to DIOR, DIOW Setup Time	15	-	
t <sub>RWPW</sub>	DIOR, DIOW Pulse Width	65	-	
t <sub>DVWL</sub>	DIOW Data Setup Time	20	-	
t <sub>DXWH</sub>	DIOW Data Hold Time	5	-	
t <sub>DVRL</sub>	DIOR Data Setup Time	15	-	
t <sub>DXRH</sub>	DIOR Data Hold Time	5	-	
t <sub>AV16L</sub>	Address Valid to IOCS16 Assertion	-	(1)	
t <sub>AX16H</sub>	Address Valid to IOCS16 Negation	-	(1)	
t <sub>AXRWH</sub>	DIOW, DIOR to Address Valid Hold Time	10	-	
t <sub>IOST</sub>	IORDY Setup Time	-	(1)	
t <sub>IOPW</sub>	IORDY Pulse Width	-	(1)	

**Note: (1) IOIS16 and INPACK is not supported.**

## 3.3.6 True IDE DMA Read/Write Access Timing (1)



Symbol	Parameter	Min	Max	Units
$t_{RWC}$	Cycle Time (Mode 2)	100	-	nsec
$t_{RWPW}$	DIOR/DIOW Pulse Width	65	-	
$t_{RDA}$	DIOR Data Access	-	50	
$t_{RWSU}$	DIOR/DIOW Data Setup Time	15	-	
$t_{WH}$	DIOW Data Hold Time	5	-	
$t_{RH}$	DIOR Data Hold Time	5	-	
$t_{DMRW}$	DMACK to DIOR/DIOW Setup Time	0	-	
$t_{RWDH}$	DIOR/DIOW to DMACK Hold Time	5	-	
$t_{RWN}$	DIOR/DIOW negated Pulse Width	25	-	
$t_{RWD}$	DIOR/DIOW to DMARQ Delay	-	35	
$t_{CSRW}$	CS(1:0) valid to DIOR/DIOW	10	-	
$t_{CSH}$	CS(1:0) Hold Time	10	-	

(1) Does not apply to FMJ drives with DMA disabled.

## 3.3.7 Refer to the PCard specifications for additional information.

## 4.0 PC Card Specifications

### 4.1 Card Information Structure (CIS)

Table 8 describes the FMJ PC Card CIS metadata. Refer to the PC Card Standard Metaformat specification for more information on the CIS metadata.

**Table 8: Card Information Structure (CIS)**

<b>Tuple</b>	<b>Description</b>
01h 03h D9h 01h FFh	Common Memory Device Information
1Ch 04h 02h D9h 01h FFh	Common Memory Operating Conditions
18h 02h DFh 01h	JEDEC programming information for Common Memory
20h 04h 00h 00h 00h 00h	Manufacturer ID String
21h 02h 04h 01h	Function class identification
22h 02h 01h 01h	Function Extensions
22h 03h 02h 04h 07h	Function Extensions
1Ah 05h 01h 07h 00h 02h 0Fh	Configuration for 16-bit CF
1Bh 0Bh C0h C0h A1h 27h 55h 4Dh 5Dh 75h 08h 00h 21h	Configuration Table Entry
1Bh 06h 00h 01h 21h B5h 1Eh 4Dh	Configuration Table Entry
1Bh 0Dh C1h 41h 99h 27h 55h 4Dh 5Dh 75h 64h F0h FFh FFh 21h	Configuration Table Entry
1Bh 06h 01h 01h 21h B5h 1Eh 4Dh	Configuration Table Entry
1Bh 12h C2h 41h 99h 27h 55h 4Dh 5Dh 75h EAh 61h F0h 01h 07h F6h 03h 01h EEh 21h	Configuration Table Entry
1Bh 06h 02h 01h 21h B5h 1Eh 4Dh	Configuration Table Entry
1Bh 12h C3h 41h 99h 27h 55h 4Dh 5Dh 75h EAh 61h 70h 01h 07h 76h 03h 01h EEh 21h	Configuration Table Entry
1Bh 06h 03h 01h 21h B5h 1Eh 4Dh	Configuration Table Entry
1Bh 04h 07h 00h 28h D3h	Configuration Table Entry
14h 00h	No-link to Common Memory
15h 16h 01h 32h 34h 38h 73h 6Fh 6Ch 69h 64h 53h 74h 61h 74h 65h 00h 32h 2Eh 35h 30h 00h FFh	Level 1 version/product information

### 4.2 ATA Commands Supported

Table 9 describes the ATA Commands supported by the FMJ PC Card. Refer to the ATA-3 specification for more information on the ATA commands.

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**Table 9: ATA Commands Supported**

Op-Code	Command Description
00h	NOP
03h	Request Sense
1Xh	Recalibrate
20h, 21h	Read Sector(s)
22h, 23h	Read Long Sector(s)
30h, 31h	Write Sector(s)
32h, 33h	Write Long Sector(s)
38h	Write Sector w/o Erase
3Ch	Write Verify Sector(s)
40h, 41h	Read Verify Sector(s)
50h	Format Track
7Xh	Seek
87h	Translate Sector
90h	Execute Device Diagnostics
91h	Initialize Device Parameters
94h, E0h	Standby Immediate
95h, E1h	Idle Immediate
96h, E2h	Standby
97h, E3h	Idle
98h, E5h	Check Power Mode
99h, E6h	Set Sleep Mode
C0h	Erase Sector
C4h	Read Multiple
C5h	Write Multiple
C6h	Set Multiple Mode
C8h, C9h	Read DMA
CAh, CBh	Write DMA
CDh	Write Multiple w/o Erase
E4h	Read Buffer
DEh	Media Lock
DFh	Media Unlock
E7h	Flush Cache
E8h	Write Buffer

**Table 9. ATA Commands Supported (continued)**

Op-Code	Command Description
ECh	Identify Device
EFh	Set Features (see 4.2.1 Set Features Sub-commands)
F5h	Wear Level



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F8h	Read Native Max Address
F8h	Set Max Address

## 4.2.1 ATA Set Feature Sub-Commands Supported

Table 10 describes the Set Feature sub-commands supported by the FMJ PC Card. Refer to the ATA-3 specification for more information on the Set Feature sub-commands.

**Table 10: Set Feature Sub-Commands Supported**

Sub-command	Description
01h	Enable 8-bit Transfer
02h	Enable Write Cache
03h	Set Transfer Mode
05h	Enable Advanced Power Management
09h	Enable Extended Power Options
0Ah	Enable Power Level 1 Commands
55h	Disable Read Look Ahead
66h	Disable reverting to power-on defaults
81h	Disable 8-bit Transfer
82h	Disable Write Cache
85h	Disable Advanced Power Management
89h	Disable Extended Power Options
8Ah	Disable Power Level 1 Commands
9Ah	Set Host Current Source Capability
AAh	Enable Read Look Ahead
BBh	4 bytes of data apply on R/W long commands
CCh	Enable revert to power-on defaults



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## 4.3 Identify Device Information

Table 11 describes the Identify Device information on the FMJ PC Card. Refer to the ATA-3 specification for more information on the Identify Device information.

**Table 11: Identify Device Information**

Word	Value	Description
Word 00	045Ah (fixed mode)	General configuration bit-significant information
	848Ah (removable mode)	15 0 = ATA device
		6 1 = Fixed Device
Word 01	XXXXh	Number of logical cylinders
Word 02	0000h	Reserved
Word 03	00XXh	Number of logical heads
Word 04	0200h	Number of unformatted bytes per track
Word 05	XXXXh	Number of unformatted bytes per sector
Word 06	XXXXh	Number of logical sectors per logical track
Words 07-08	XXXXh XXXXh	Number of sectors per device
Word 09	0000h	Reserved
Words 10-19	Vendor Specific	Serial number (20 ASCII characters)
Word 20	0002h	Buffer Type = Dual ported multi-sector buffer
Word 21	0001h	Buffer Size = 512 bytes
Word 22	0004h	4 ECC bytes passed on r/w long commands
Words 23-26	Vendor Specific	Firmware revision (8 ASCII characters)
Words 27-46	Vendor Specific	Model number (40 ASCII characters)
Word 47	8001h	15-8 80h
		7-0 00h = Reserved
		01h-FFh = Maximum number of logical sectors that shall be transferred per DRQ data block on R/W MULT commands
Word 48	0000h	Double Word (32-bit) not supported
Word 49	0F00h	Capabilities
		15-14 Reserved.
		13 1 = Standby timer values as specified in this standard are supported
		12 Reserved.
		11 1 = IORDY supported
		10 1 = IORDY may be disabled
		9 1 = LBA supported
		8 1 = DMA supported
		7-0 Retired
Word 50	0000h	Reserved
Word 51	0200h	15-8 PIO data transfer cycle timing
Word 52	0000h	15-8 DMA data transfer cycle timing
<b>Word</b>	<b>Value</b>	<b>Description</b>
Word 53	0007h	15-3 Reserved





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		2 1 = the fields reported in word 88 are valid
		1 1 = the fields reported in words (64-70) are valid
		0 1 = the fields reported in words (54-58) are valid
Word 54	XXXXh	Current Number of current logical cylinders
Word 55	XXXXh	Current Number of current logical heads
Word 56	XXXXh	Number of current Logical Sectors per track
Words 57-58	XXXXh XXXXh	Current Capacity in Sectors
Word 59	010Xh	Current Sectors per R/W multiple
		15-9 Reserved
		8 1 = Multiple sector setting is valid
		7-0 10h = Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE Multiple commands
Words 60-61	XXXXh XXXXh	Total number of user addressable logical sectors
Word 62	0000h	Single word DMA modes supported
Word 63	XX07h	15-11 Reserved
		10 1 = Multiword DMA mode 2 is selected
		0 = Multiword DMA mode 2 is not selected
		9 1 = Multiword DMA mode 1 is selected
		0 = Multiword DMA mode 1 is not selected
		8 1 = Multiword DMA mode 0 is selected
		0 = Multiword DMA mode 0 is not selected
		7-3 Reserved
		2 1 = Multiword DMA mode 2 and below are supported
		1 1 = Multiword DMA mode 1 and below are supported
		0 1 = Multiword DMA mode 0 is supported
Word 64	0003h	15-8 Reserved
		7-0 PIO modes 1 to 4 supported
Word 65	0078h	Minimum Multiword DMA transfer cycle time per word
		15-0 Cycle time in nanoseconds
Word 66	0078h	Manufacturer's recommended Multiword DMA cycle time
		15-0 Cycle time in nanoseconds
Word 67	0078h	Minimum PIO transfer cycle time without flow control
		15-0 Cycle time in nanoseconds
Word 68	0078h	Minimum PIO transfer cycle time with IORDY flow control
		15-0 Cycle time in nanoseconds

Word	Value	Description
Word 80	0003h	Major version number
		15-9 Reserved



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		8 0 = supports ATA8-ACS
		7 0 = supports ATA/ATAPI-7
		6 0 = supports ATA/ATAPI-6
		5 0 = supports ATA/ATAPI-5
		4 0 = supports ATA/ATAPI-4
		3 1 = supports ATA/ATAPI-3
		2 1 = supports ATA/ATAPI-2
		1 1 = supports ATA/ATAPI-1
		0 Reserved
Word 88	XX00h	Ultra DMA modes
		15 Reserved
		14 1 = Ultra DMA mode 6 is selected
		0 = Ultra DMA mode 6 is not selected
		13 1 = Ultra DMA mode 5 is selected
		0 = Ultra DMA mode 5 is not selected
		12 1 = Ultra DMA mode 4 is selected
		0 = Ultra DMA mode 4 is not selected
		11 1 = Ultra DMA mode 3 is selected
		0 = Ultra DMA mode 3 is not selected
		10 1 = Ultra DMA mode 2 is selected
		0 = Ultra DMA mode 2 is not selected
		9 1 = Ultra DMA mode 1 is selected
		0 = Ultra DMA mode 1 is not selected
		8 1 = Ultra DMA mode 0 is selected
		0 = Ultra DMA mode 0 is not selected
		7 Reserved
		6 0 = Ultra DMA mode 6 and below are not supported
		5 0 = Ultra DMA mode 5 and below are not supported
		4 0 = Ultra DMA mode 4 and below are not supported
		3 0 = Ultra DMA mode 3 and below are not supported
		2 0 = Ultra DMA mode 2 and below are not supported
		1 0 = Ultra DMA mode 1 and below are not supported
		0 0 = Ultra DMA mode 0 is not supported
Word 163	0000h	Multiword DMA mode 4 and PIO mode 6 are not supported

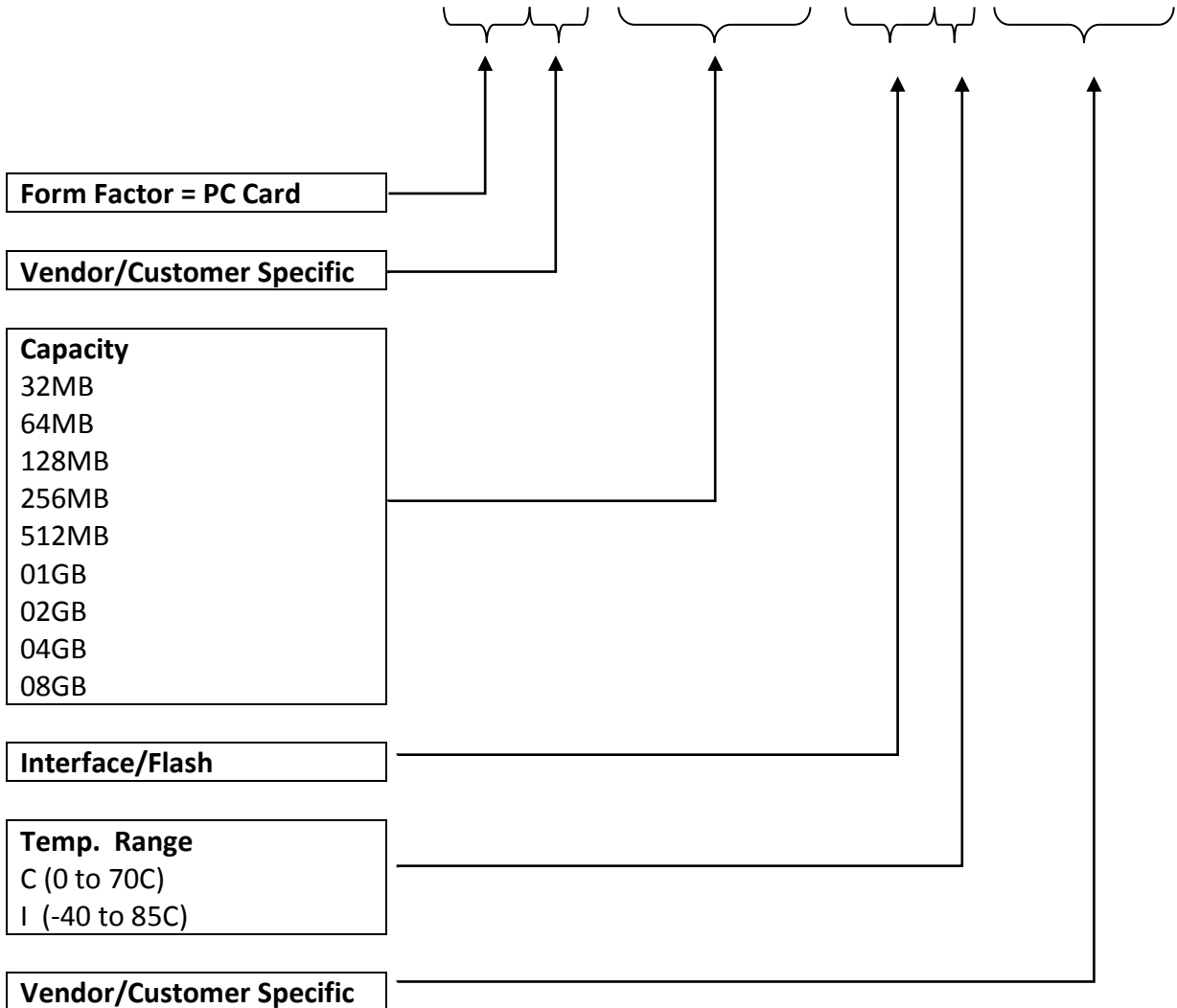
## 5.0 Ordering Information

The following describes the part number ordering nomenclature from FMJ Storage.



# FMJ LG PC Card

## ATV-08GB-TSI-0002



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1 Megabyte (MB) equals 1 Million Bytes; 1 Gigabyte (GB) equals 1 Billion Bytes. Accessible capacity may vary depending on the operating environment.

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